

Exploring Benefits and Designs of Optically Connected Disintegrated Processor Architecture

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The logo for KAIST (Korea Advanced Institute of Science and Technology), consisting of the letters "KAIST" in a bold, blue, sans-serif font, with a blue horizontal swoosh underneath.

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Motivation

➤ Motivation

- OCDP Architecture
- Power Comparison
- Conclusion

- ▶ Transistor density grows exponentially
- ▶ But, processors are physically constrained
 - Low yield, bandwidth wall, power wall
 - *Dark silicon*: we can build dense devices we cannot afford to power
- ▶ **Optically-Connected Disintegrated Processor (OCDP)**
 - Divide (impractical) monolithic processor into chiplets
 - Improves yield
 - Breaks the bandwidth wall
 - **Breaks the power wall**
 - Spread out chiplets, cheaper cooling



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- ▶ Advantage of nanophotonics
 - Latency
 - Bandwidth density
- ▶ Using nanophotonics for inter-chip interconnect
 - Reduced memory latency
 - Increased off-chip bandwidth
 - Increased total chip area
 - Increased power budget
- ▶ Analytical model* for performance estimation

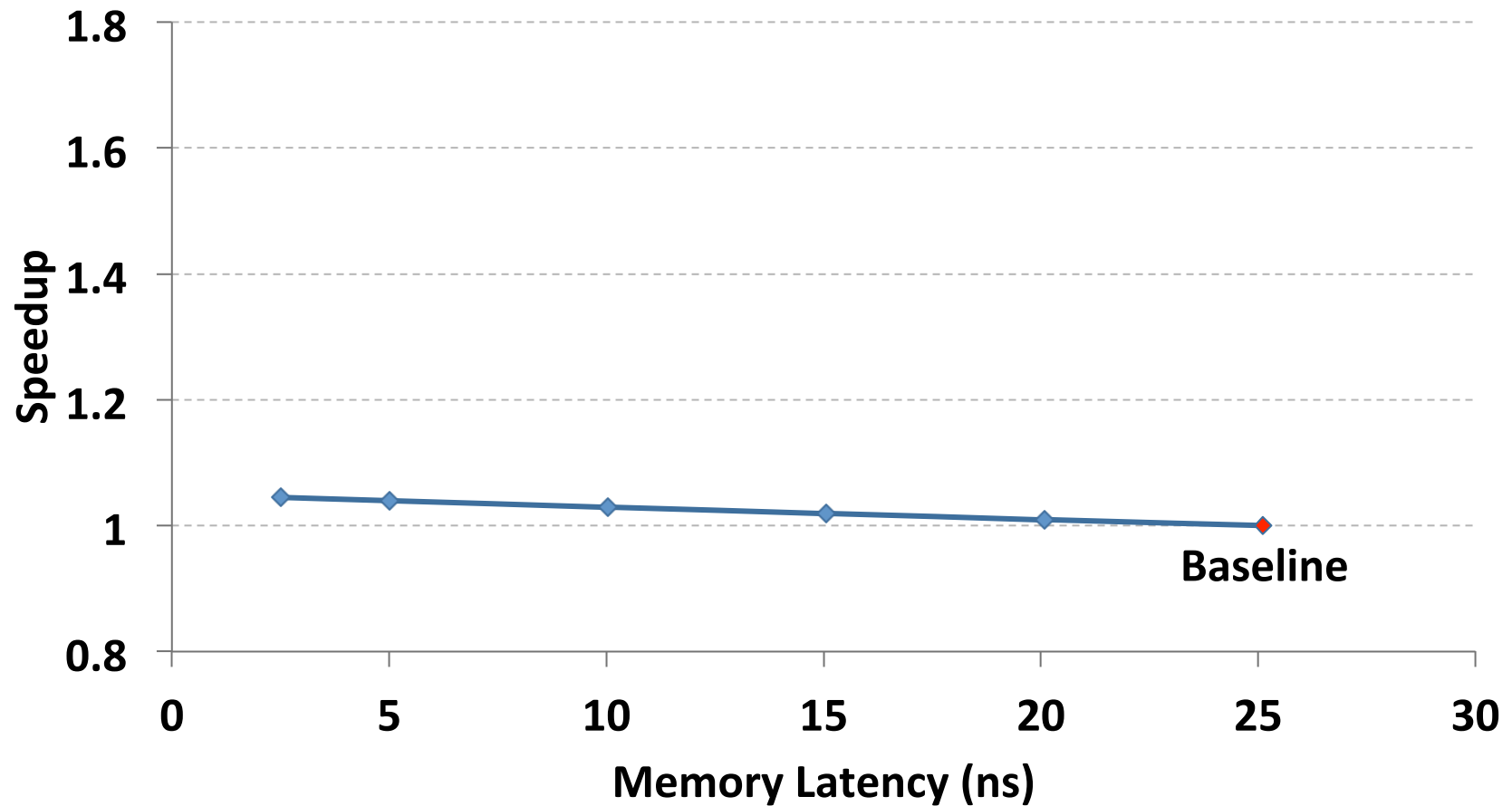
* N. Hardavellas et al., Tech Report NWU-EECS-10-05, Mar. 2010.



Memory Latency

➔ Motivation

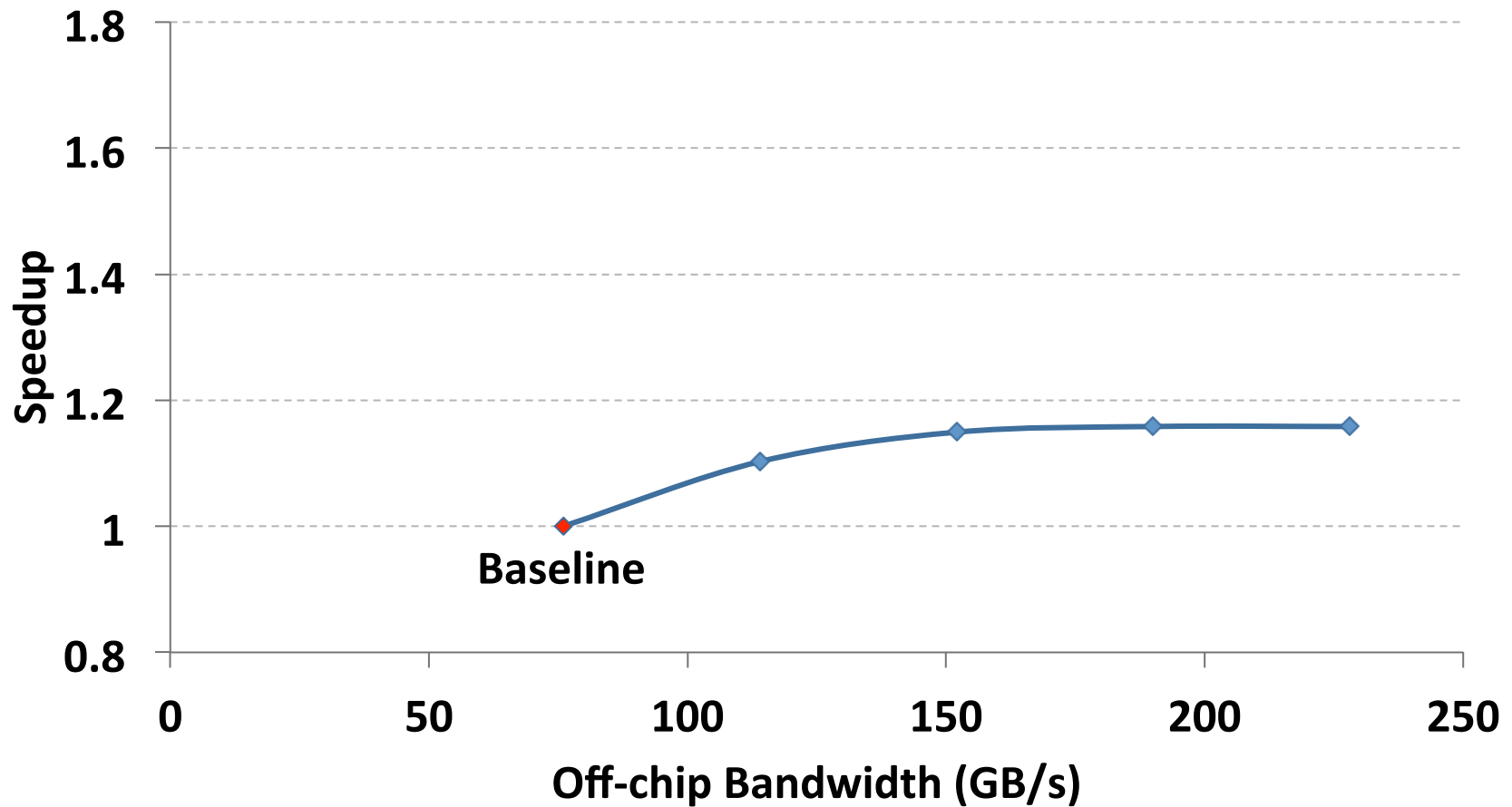
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Off-chip Bandwidth

➔ Motivation

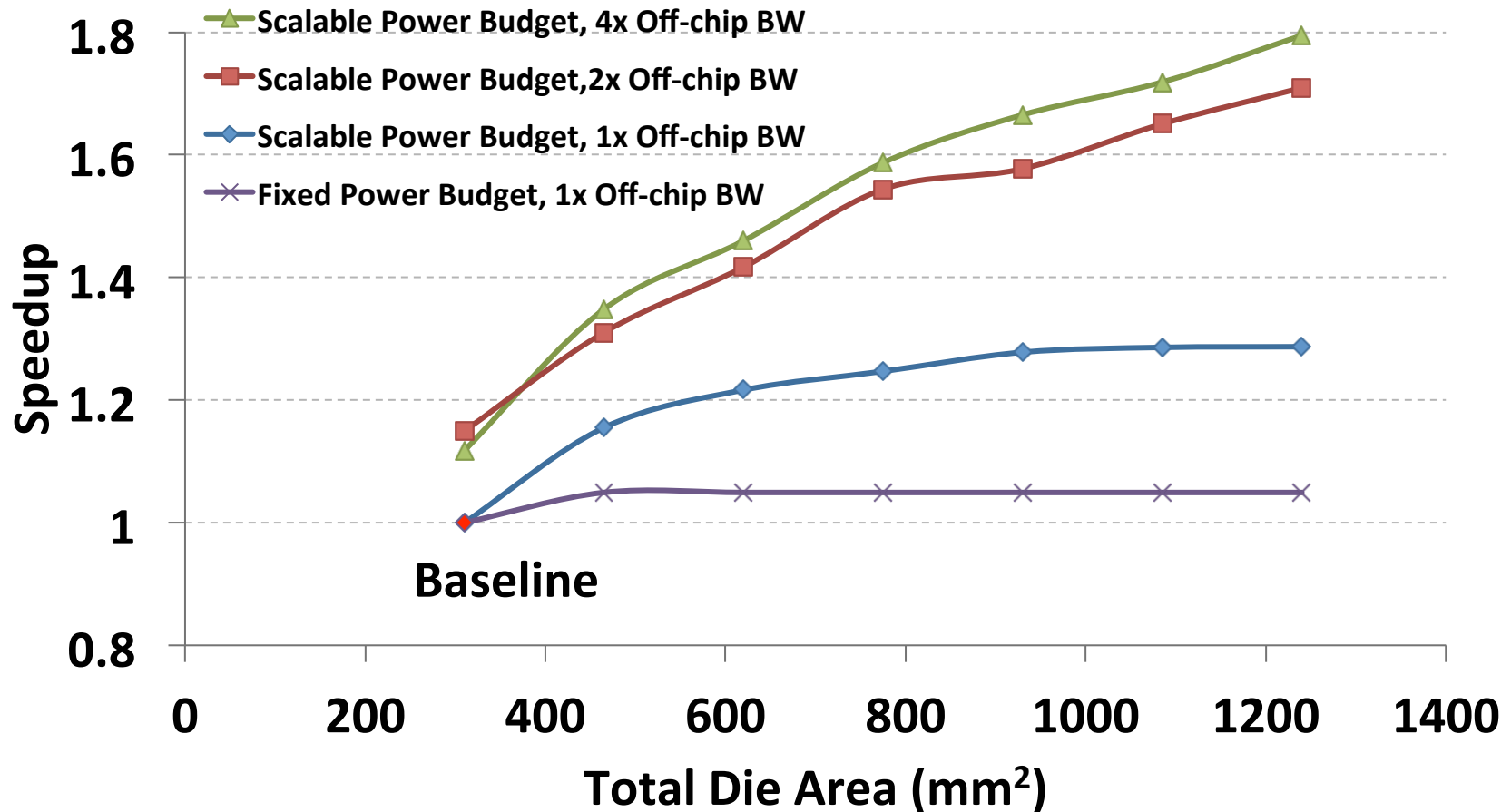
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Scaling Power, Chip Area

Motivation

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Motivation

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- ▶ Performance impact
 - Reduced memory latency → minimal
 - Improved off-chip bandwidth → small
 - Total chip area → small
 - **Power budget → big**
- ▶ Power budget scalability is critical
 - Spread out chiplets
 - Cheaper cooling
- ▶ **Optically-Connected Disintegrated Processor (OCDP)**



Off-chip Optical Channels

➔ Motivation

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Material	Optical Loss	Propagation Speed	Pitch (density)
Silicon Waveguide	0.3 dB/cm [*]	0.286c	20um
Optic Fiber	0.2 dB/km	0.676c	250um

- ▶ Optical fiber is low-loss, high speed
 - Enables further spreading out chiplets
 - *BW density was a challenge*

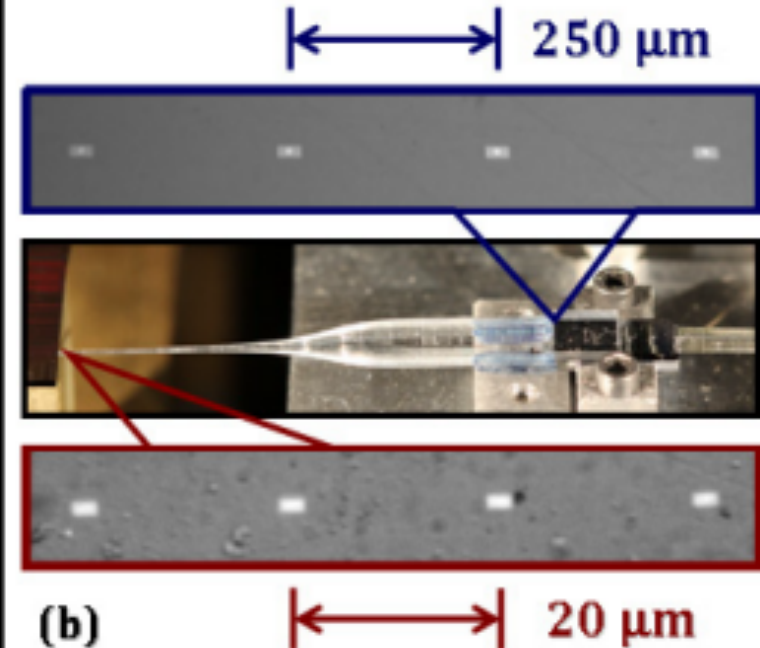
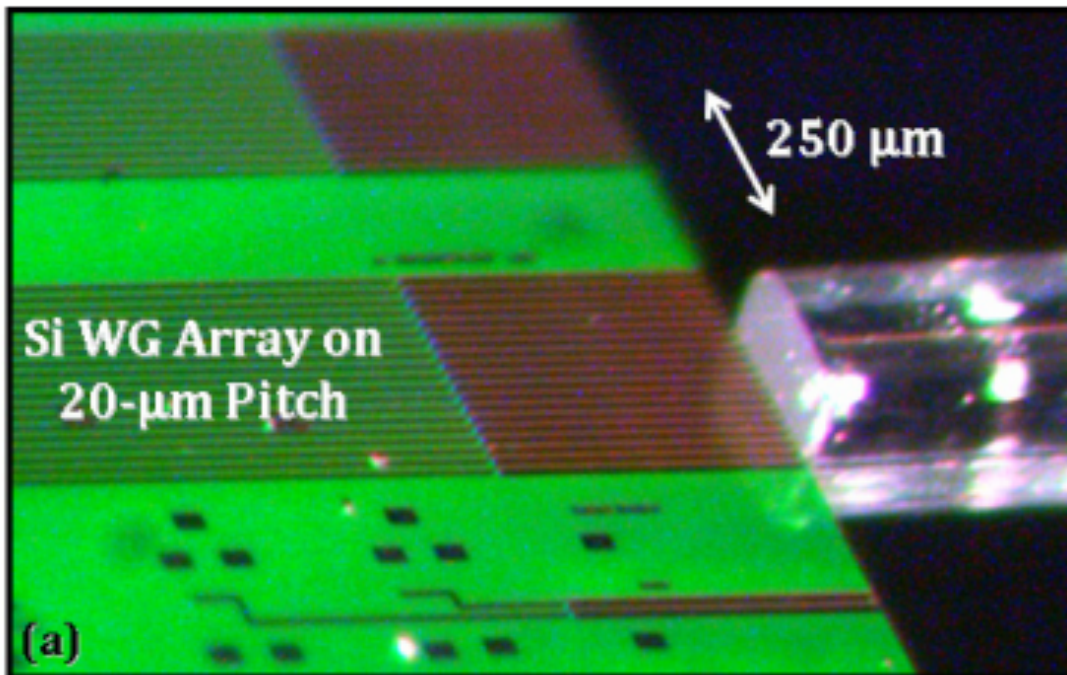
* J. Cardenas et al., Optics Express 2009



Dense Off-chip Coupling

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- ▶ Dense optical fiber array [Lee et al., OSA/OFC/NFOEC 2010]
- ▶ <1dB loss, 8 Tbps/mm demonstrated



OCDP Design Considerations

➤ Motivation

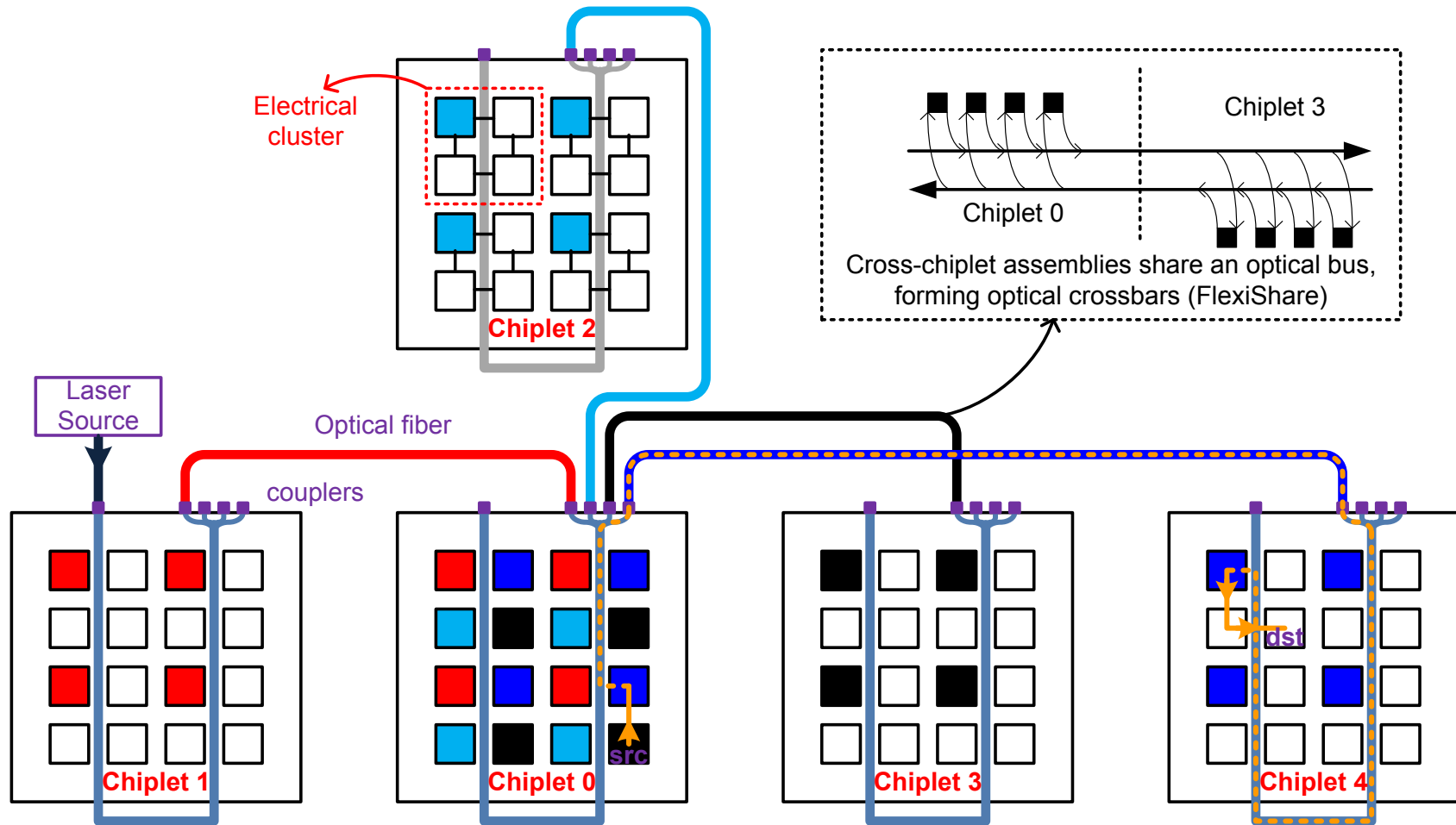
- OCDP Architecture
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- ▶ Inter-chiplet optical channel technology
 - Optic fiber for low loss
- ▶ Inter-chiplet optical channel organization
 - Point-to-point [Koka et al., ISCA 2010]
 - Minimize waveguide and coupler loss
- ▶ On-chip topology
 - Scalable chiplet size
- ▶ *On-chip / off-chip bandwidth interfacing*
 - Distributed BW, seamless integration



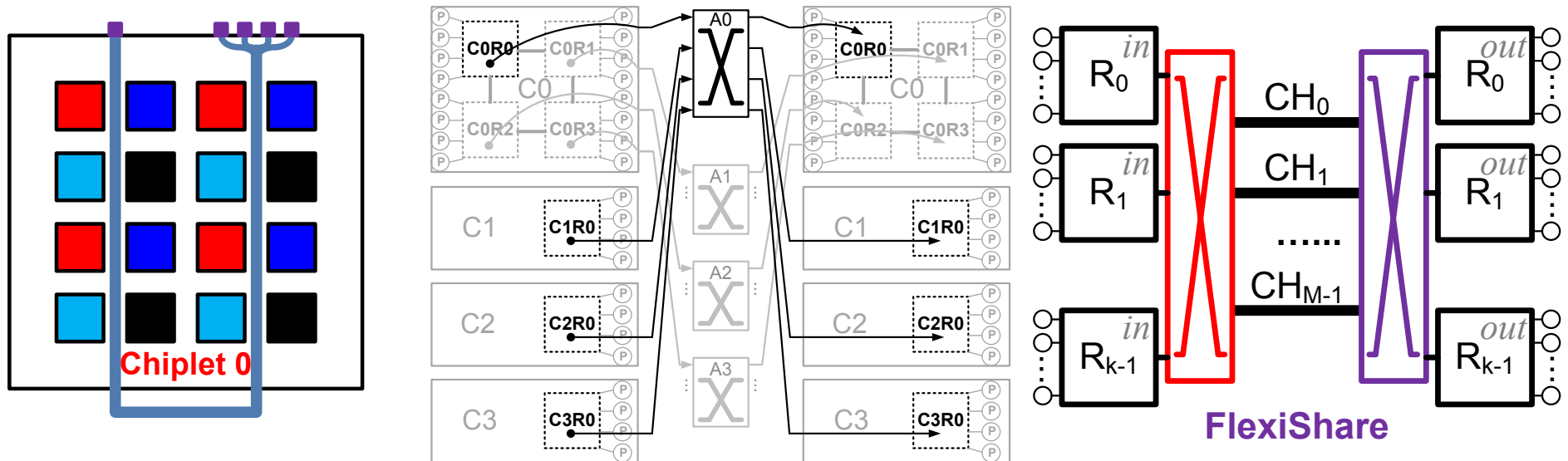
OCDP Architecture

- Motivation
- ➔ **OCDP Arch.**
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Firefly On-chip Topology

- Motivation
- **OCDP Arch.**
- Power Comparison
- Conclusion

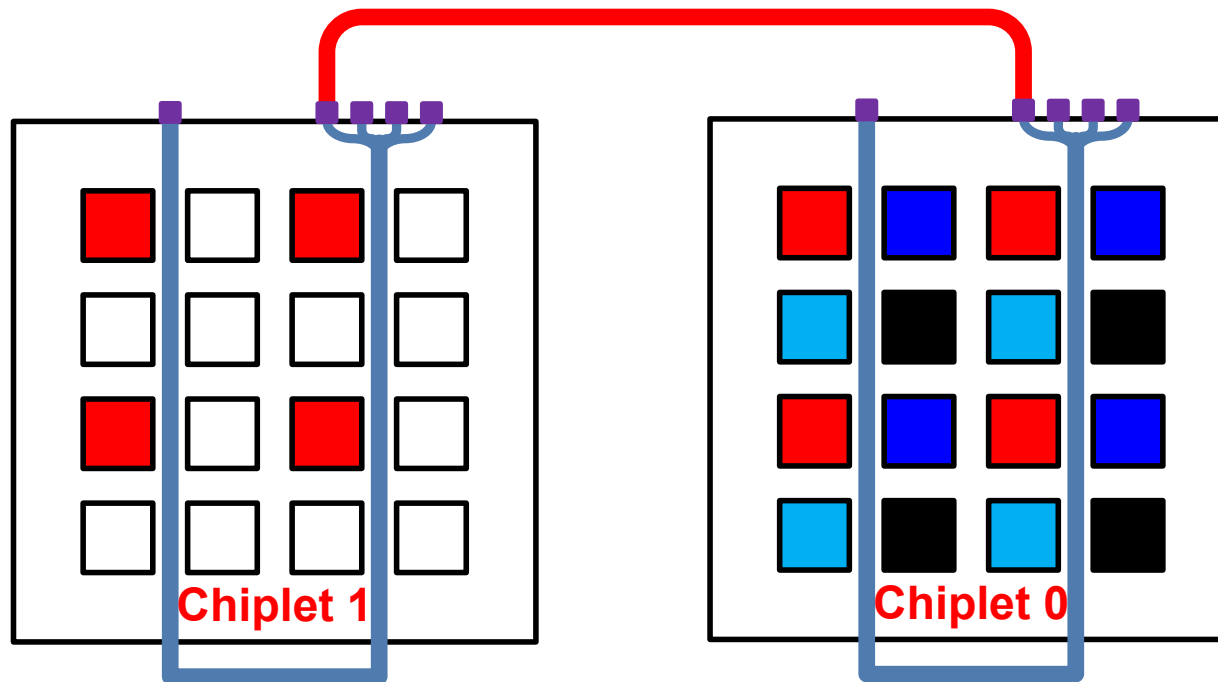


- ▶ **Firefly** on-chip topology [Pan et al., ISCA 2009]
 - Flexible chiplet sizing, optical on-chip communication
- ▶ **FlexiShare** optical crossbars [Pan et al., HPCA 2010]
 - Flexible bandwidth provisioning
 - Light-weight optical arbitration needed, proposed



Extending across chiplets

- Motivation
- **OCDP Arch.**
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- ▶ Distributed bandwidth across chiplets
- ▶ Flexible inter-chiplet bandwidth provisioning
- ▶ Minimal number of couplers
- ▶ Seamless on-chip/off-chip interfacing



Technology Assumptions

- Motivation
- OCDP Architecture
- **Power Eval.**
- Conclusion

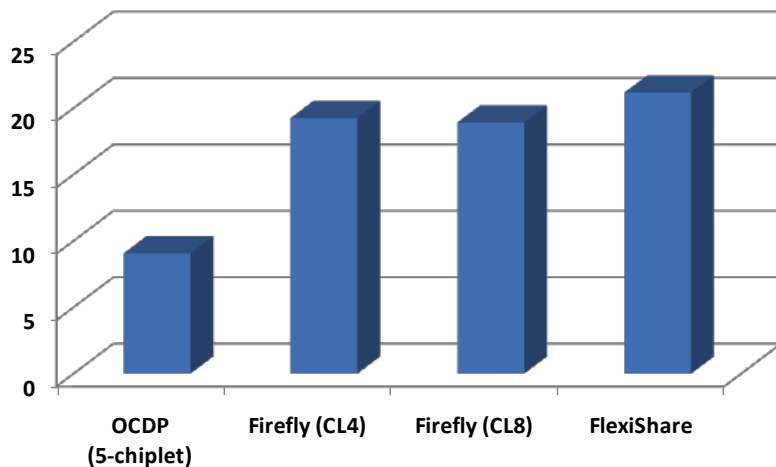
Parameter	Loss	Parameter	Value
Coupler	1 dB	Detector Sensitivity	0.01 mW
Splitters	1 dB	DWDM	16 λ
Non-linear	1 dB	fiber coupler loss	0.1
Modulator Insertion	0.1 dB	fiber loss	2.00E-06 dB/cm
Waveguide	0.3 dB/cm	ring heating power	40 μ W/ring
Ring Through	0.001 dB	Modulation Power	80 fJ/bit
Filter Drop	1.5 dB	Demodulation Power	40 fJ/bit
PhotoDetector	0.1 dB		

► Moderate DWDM (16-way)

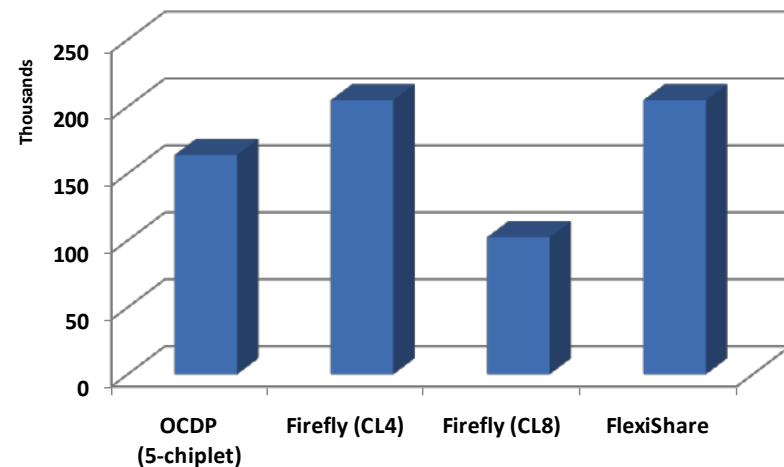
Optical Power (320-core)

- Motivation
- OCDP Architecture
- **Power Eval.**
- Conclusion

Total Optical Loss (dB)



Total Number of Ring Resonators

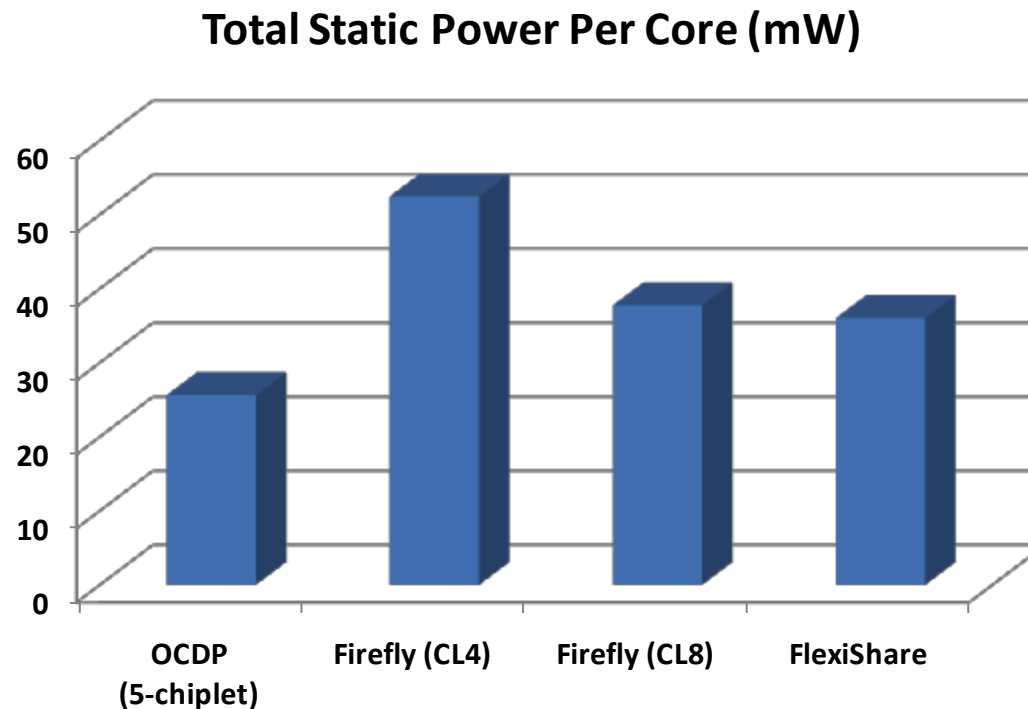


- ▶ 5-chiplet OCDP vs. single-chip topologies
- ▶ Total number of optical channels (wavelengths) held constant.



Per-Core Network Static Power

- Motivation
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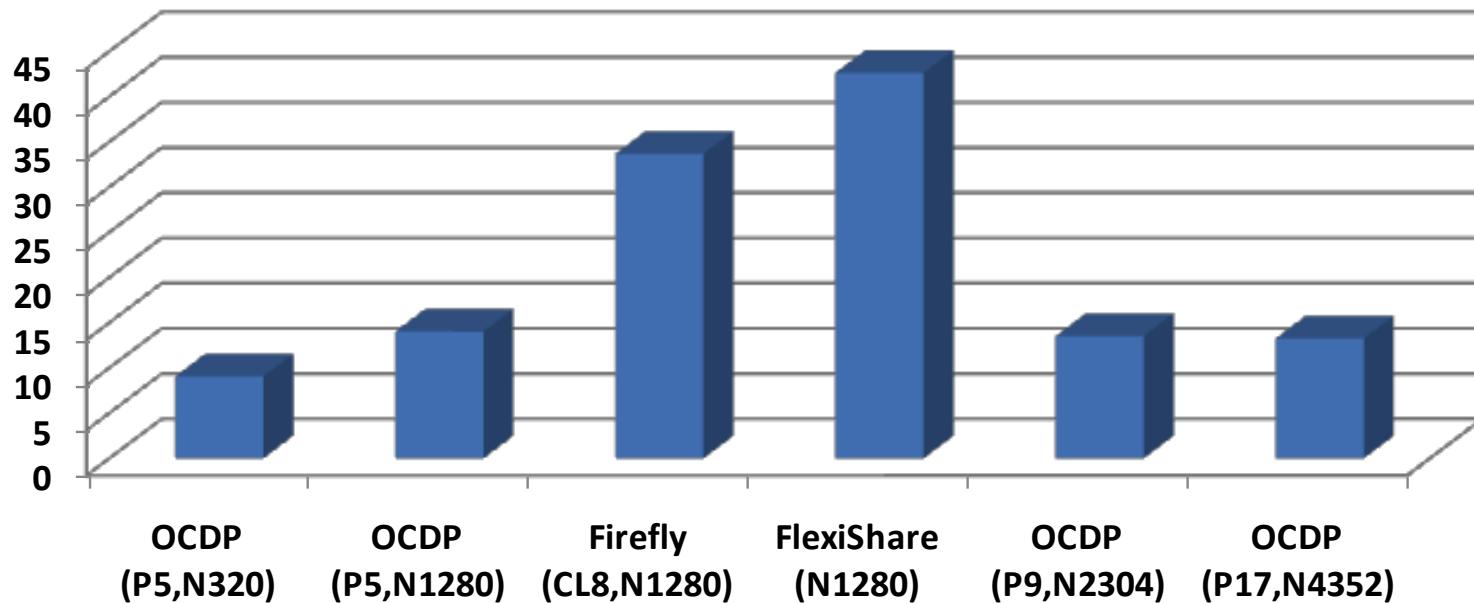
- ▶ ~ 30% power reduction compared to the best alternative.



Scaling Up

- Motivation
- OCDP Architecture
- **Power Eval.**
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Total Optical Loss (dB)

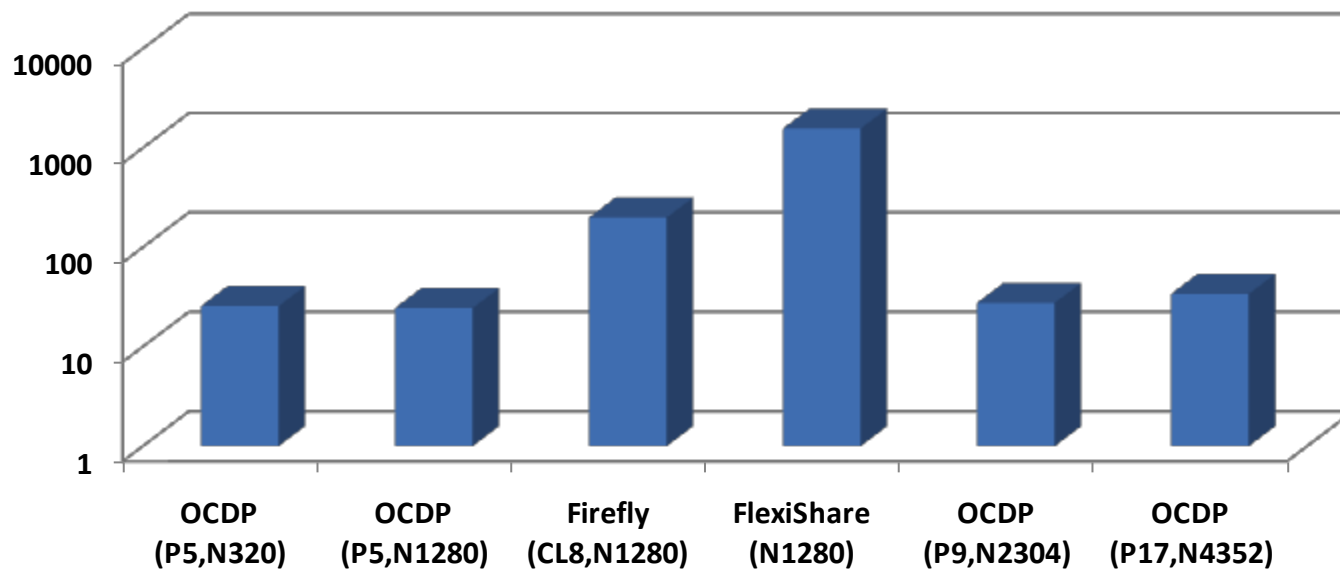


- ▶ OCDP limits the total on-chip waveguide length
- ▶ Better optical scalability

Scaling Up

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Total Static Power Per Core (mW)



- ▶ OCDP shows very good power scalability.
- ▶ Single-chip is impractical for 1280-core processor



Conclusion

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- ▶ **OCDP leverages**
 - Low latency / high bandwidth density
 - Low loss optic fibers
- ▶ **Power scalability is critical**
 - Minimize optical loss on the path
- ▶ **Seamless on-chip / off-chip interfacing**
 - Firefly intra-chiplet (distributed off-chiplet BW)
 - Point-to-point (Dragonfly) inter-chiplet
- ▶ **Performance evaluation needed**
- ▶ **Chiplet composition to be explored**



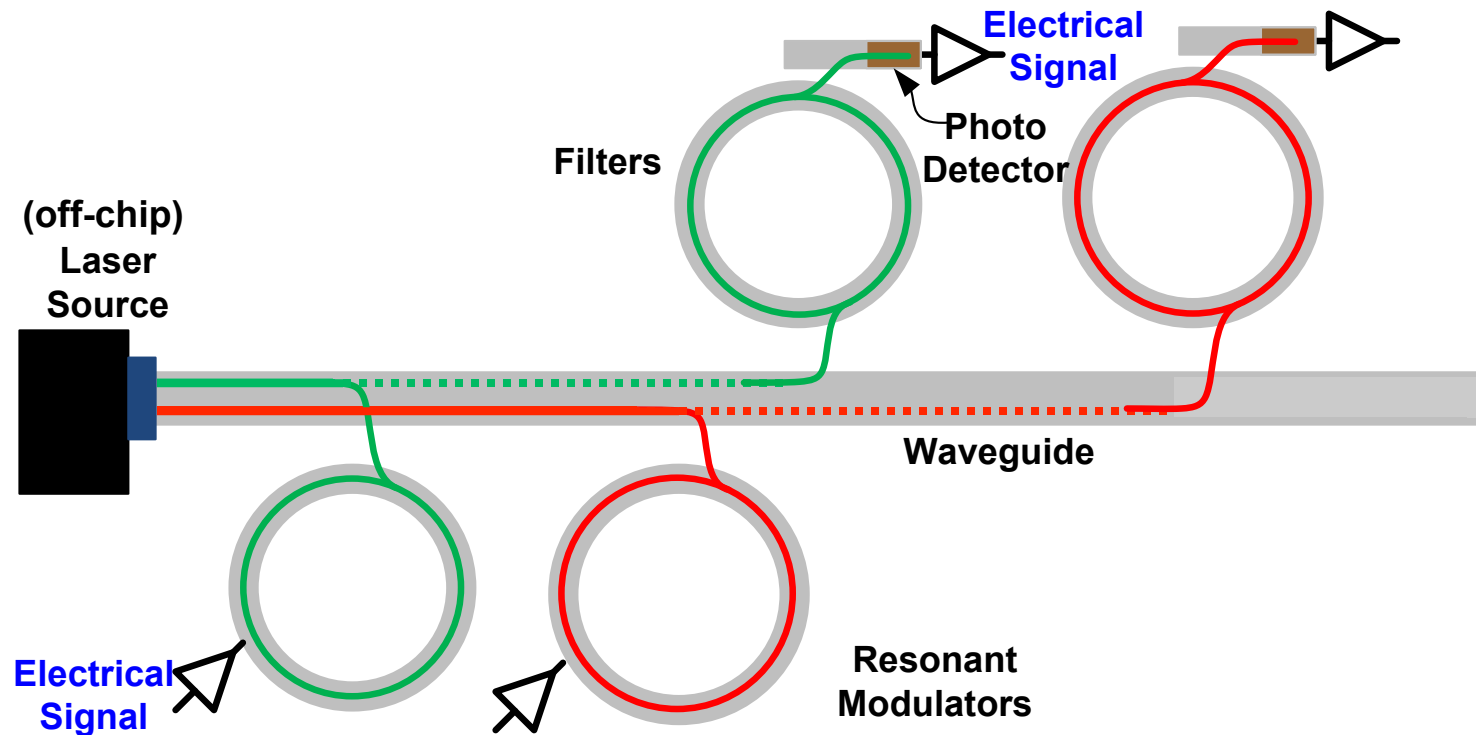
Questions?

THANK YOU!

On-chip Optical Channel

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▶ Silicon photonics with DWDM