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CS/ECE Distinguished Lecturer Series

Extracting Thread-level Parallelism on Simultaneous Multithreaded Processors

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Abstract:

Simultaneous multithreading is a processor design that combines hardware multithreading with superscalar processor technology to allow multiple threads to issue instructions each cycle. Unlike other multithreaded architectures, in which only a single hardware context (i.e., thread) is active on any given cycle, SMT permits all thread contexts to simultaneously compete for and share processor resources. Unlike conventional superscalar processors, which suffer from a lack of per-thread instruction-level parallelism, simultaneous multithreading uses multiple threads to compensate for low single-thread ILP. The performance consequence is significantly higher instruction throughput and program speedups on a variety of workloads that include commercial databases, web servers and scientific applications in both multiprogrammed and parallel environments. SMT technology has been successfully transferred to the commercial sector. Several chip manufacturers have announced SMT products; others are still in the design phase of product development. Over the past few years we have done SMT-related research in several different areas that include microarchitectural design, and compiler and operating systems support for SMT. In this talk I will cover the two most recent efforts, mini-threads and instruction speculation.

Bio:

Susan Eggers is a Professor in the Department of Computer Science and Engineering at the University of Washington. She received her doctorate in Computer Science at the University of California, Berkeley, in 1989. Her research interests encompass multiple areas within computer architecture and compilation, all with an emphasis on experimental performance analysis. Her current work is on issues in processor design and dynamic optimization. In 1989 she was awarded an IBM Faculty Development Award and in 1990 an NSF Presidential Young Investigator Award. She is a Fellow of the ACM and IEEE, and a member of the NSF CISE Advisory Committee and the Scientific Advisory Board of Equator Technologies, Inc.