EECS 213: Homework 3

Memory and Cache

Spring 2007

Important Dates

Due: May 18, 2007 (11:59PM)

Submitting your homework: Please use the course submission site. There is a link to it from the class site. Submit only ASCII text files.

To be done individually.

1. Consider a processor which uses 16 bit addresses and can address \(2^{16} = 64K\) bytes of memory. Suppose that it has one level of cache. As in Figure 6.25 of your textbook, the address is split into a \(t\) bit tag, an \(s\) bit set index, and a \(b\) bit block offset. The cache consists of 1024 bytes, with a block size of 32 bytes. Answer each of the following for direct-mapped, 4-way set associative, and fully associative versions of the cache.

   (a) How many cache lines are there?
   (b) What is \(b\)?
   (c) What is \(s\)?
   (d) What is \(t\)?

2. For the cache in problem 1, draw the cache given it is structured as follows. You can elide replicated components, but annotate your drawing with how many components there are.

   (a) Direct-mapped
   (b) 4-way set associative
   (c) Fully associative

3. Our company wants to optimize the performance of the following code

   ```c
   void vector_add(int n, int *a, int *b, int *c)
   {
       int i;
   ```
for (i=0; i<n; i++) {
    c[i] = a[i] + b[i];
}

...